Waveform Generator Bit Fields

Application Note 04 Monday, July 19, 2021

The ARC420 timing board contains circuitry that writes 16-bit data words to the controller backplane over the pins SS15 ~ SS0 ('SS' for Signal State) at a maximum rate of 50 MHz, or every 20 ns. The twelve least significant signals SS11 ~ S0 are connected to the twelve clock drivers on the ARC430 board, while SS1 ~ SS0 are used by the video processor. The four most significant bits SS15 ~ SS12 are used for addressing the video or clock driver board and for selecting some special functions described below. The current data word is written to the backplane immediately, while a 16 bit word linked to each data word causes a delay until the next data word is written. The delay time is 20 ns times the 16-bit delay number, which is the same time it takes to write a single data word.

Several data and delay words are associated, and called a waveform array. When the FPGA is instructed by the micro-controller to execute a waveform array it reads the first word in the array and stores is as the number of values in the array. It then reads the next value, process it, and continues reading each value in sequence and loops back to the starting value when it has processed the number of values in the array. It will repeat this looping by the number supplied as the loop counter by the micro-controller. These waveform arrays are compiled from the micro-controller source code and written to the FPGA after the micro-controller software is download to the controller from the host computer. The set of all waveform arrays is called a waveform table in our documentation.

A second block of memory in the FPGA is a FIFO (First In First Out) memory that contains the addresses of each waveform array to be executed, along with the associated loop counter. Ten bits are assigned to the address and 22 bits to the loop counter. This FIFO is 512 words deep, and is named the command FIFO. The micro-controller writes commands to the command FIFO that will get executed in the order in which they were written. The command is lost after it is executed, as the FIFO advances to the next command. The micro-controller needs to write commands fast enough that the FIFO is never empty, but not so much that it gets full.

Micro-controller source code

Two files in the supplied micro-controller source code are of interest here. The *.waveforms file generates the waveform arrays and writes to the video and clock driver DACs. It is similar in concept to the Gen III waveform files, though here it is interpreted by a C compiler rather than a DSP assembler. The second file, named HxRG.c (or similar) contains the code whose main job is to supply the waveform generator command FIFO with commands. It controls the exposure, and the array readout and idling. Developers and system integrators will devote most of their attention to these two files.

The tables below describe the meaning of the bit fields of the 32-bit waveform generator words.

Video Processor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	x	x	x	x	x	x	x	x	x	x	XFER	ADC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dly15	Dly14	Dly13	Dly12	Dly11	Dly10	Dly09	Dly08	Dly07	Dly06	Dly05	Dly04	Dly03	Dly02	Dly01	Dly00

This will write the XFER and ADC bits to the video processing boards if the corresponding mask bit is cleared. A low to high transition of ADC will start the A/D conversion. The A/D datum will be read by the video processor FPGA if XFER is set, and be discarded if cleared. The ADC conversion takes 200 ns, and an additional 40 ns is required for the FPGA to read the datum, giving a minimum pixel time of 240 ns. The A/D acquisition time is 85 ns. The delay function executes are described above.

Clock Driver

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	SS11	SS10	SS09	SS08	SS07	SS06	SS05	SS04	SS03	SS02	SS01	SS00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dly15	Dly14	Dly13	Dly12	Dly11	Dly10	Dly09	Dly08	Dly07	Dly06	Dly05	Dly04	Dly03	Dly02	Dly01	Dly00

The bits SS11 ~ SS00 are written to the clock driver circuits CLKOUT11 ~ CLKOUT0 if the corresponding mask bit is cleared. The delay function executes are described above.

Signal Averaging

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	NSA5	NSA4	NSA3	NSA2	NSA1	NSA0	P04	P03	P02	P01	P00	XFER	0	0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Dly15	Dly14	Dly13	Dly12	Dly11	Dly10	Dly09	Dly08	Dly07	Dly06	Dly05	Dly04	Dly03	Dly02	Dly01	Dly00

Start a series of signal averaging A/D converter cycles. Free running A/D pulses will be stopped during this operation, and re-started afterwards.

XFER is set to average and transfer image data, cleared to discard them.
P04 ~ P00 times 20 ns is the period of the start A/D pulses. 0xC => 240 ns is the minimum.
NSA5 ~ NSA0 is the number of A/D converter pulses per pixel that will be generated.
P = (NS+1) should be entered in the delay field Dly15 ~ Dly00 to delay the next WG instruction from executing until this one is complete.

Mask Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	v	MR11	MR10	MR09	MR08	MR07	MR06	MR05	MR04	MR03	MR0	MR01	MR00

There is circuitry in the waveform generator on the ARC420 that prevents selected bits of the 16-bit data word to not be written to the backplane, while writing the non-selected bits. A bit in the data word is selected for not being written to, or masked, by writing setting the corresponding bit in the mask register. If y = 0 the bits MR11 ~ MR00 are written to the video board mask register, and if y = 1 they are written to the clock driver mask register. Examples are shown in the waveforms file for the READ Enable and RESET enable functions and when using the HxRG serial interface.

Start the free running A/D converter start pulses

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00

Stop the free running A/D converter start pulses

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	x	x	x	x	x	x	x	x	x	x	x

The A/D converters on the video boards exhibit a bit of drift if their duty cycle is changed appreciably. This can happen when the system changes from exposing to reading out, or from slow to fast clocking. Much of this drift is caused by slight changes in the reference voltage that is input to the converter. While this circuit has been implemented following the manufacturer's recommendations, an additional precaution is implemented by having the A/D converter free running with a separate circuit when it's not being used on real pixels. The XFER bit described above in the video processor section allows the A/D converter to generate output numbers that are not processed. P10 ~ P00 is the number of 20 ns multiples of the time between A/D start pulses.